AMENDMENTS TO THE CLAIMS

1. (Original) At least one pixel cell comprising:

a semiconductor substrate including a strained silicon layer at an upper portion thereof; and

a photosensor for generating charge formed in an upper region of said semiconductor substrate.

2. (Original) The pixel cell of claim 1, wherein said strained silicon layer has a thickness of about 500Å to about 1000Å.

3. (Original) The pixel cell of claim 1, wherein said strained silicon layer comprises a top silicon layer formed over a silicon-germanium base layer.

4. (Original) The pixel cell of claim 3, wherein said silicon-germanium base layer comprises $Si_XGe_{(1-X)}$.

5. (Original) The pixel cell of claim 3, wherein said silicon-germanium base layer comprises $Si_XGe_YC_Z$, and $X+Y+Z = 1$.

6. (Original) The pixel cell of claim 3, wherein said silicon-germanium base layer comprises multiple layers of silicon-germanium having varying concentrations of germanium.

7. (Original) The pixel cell of claim 3, wherein said silicon-germanium base layer has a germanium concentration of about 30% to about 40%.

8. (Withdrawn) The pixel cell of claim 1, further comprising a reset transistor, a source follower transistor, and a row select transistor formed in regions of said substrate containing said strained layer.

9. (Withdrawn) The pixel cell of claim 8, further comprising a transfer transistor formed in a region of said substrate containing said strained silicon layer.

10. (Withdrawn) At least one pixel cell comprising:

a semiconductor substrate including a strained silicon layer at an upper portion;

a photosensor for generating charge formed in an upper region of said semiconductor substrate;

a reset transistor formed in association with said upper portion of said semiconductor substrate;

a source follower transistor formed in association with said upper portion of said semiconductor substrate; and

a row select transistor formed in association with said upper portion of said semiconductor substrate.

11. (Withdrawn) The pixel cell of claim 10, wherein said strained silicon layer has a thickness of about 500Å to about 1000Å.

12. (Withdrawn) The pixel cell of claim 10, wherein said strained silicon layer comprises a top silicon layer formed over a silicon-germanium base layer.

13. (Withdrawn) The pixel cell of claim 12, wherein said silicon-germanium base layer comprises $Si_XGe_{(1-X)}$.

14. (Withdrawn) The pixel cell of claim 12, wherein said silicon-germanium base layer comprises $Si_XGe_YC_Z$, and $X+Y+Z = 1$.

15. (Withdrawn) The pixel cell of claim 12, wherein said silicon-germanium base layer comprises multiple layers of silicon-germanium having varying concentrations of germanium.

16. (Withdrawn) The pixel cell of claim 12, wherein said silicon-germanium base layer has a germanium concentration of about 30% to about 40%.

17. (Withdrawn) At least one pixel cell comprising:

a semiconductor substrate including a strained silicon layer at an upper portion;

a photosensor for generating charge formed in an upper region of said semiconductor substrate;

a reset transistor formed in association with said upper portion of said semiconductor substrate;

a source follower transistor formed in association with said upper portion of said semiconductor substrate;

a row select transistor formed in association with said upper portion of said semiconductor substrate; and

a transfer transistor formed in association with said upper portion of said semiconductor substrate.

18. (Withdrawn) The pixel cell of claim 17, wherein said strained silicon layer has a thickness of about 500Å to about 1000Å.

19. (Withdrawn) The pixel cell of claim 17, wherein said strained silicon layer comprises a top silicon layer formed over a silicon-germanium base layer.

20. (Withdrawn) The pixel cell of claim 19, wherein said silicon-germanium base layer comprises $Si_XGe_{(1-X)}$.

21. (Withdrawn) The pixel cell of claim 19, wherein said silicon-germanium base layer comprises $Si_XGe_YC_Z$, and $X+Y+Z = 1$.

22. (Withdrawn) The pixel cell of claim 19, wherein said silicon-germanium base layer comprises multiple layers of silicon-germanium having varying concentrations of germanium.

23. (Withdrawn) The pixel cell of claim 19, wherein said silicon-germanium base layer has a germanium concentration of about 30% to about 40%.

24. (Withdrawn) An imager comprising: a plurality of pixel cells, at least one of said pixel cells comprising:

a semiconductor substrate including a strained silicon layer at an upper portion; and

a photosensor for generating charge formed in an upper region of said semiconductor substrate.

25. (Withdrawn) The imager of claim 24, wherein said strained silicon layer has a thickness of about 500Å to about 1000Å.

26. (Withdrawn) The imager of claim 24, wherein said strained silicon layer comprises a top silicon layer formed over a silicon-germanium base layer.

27. (Withdrawn) The imager of claim 26, wherein said silicon-germanium base layer comprises $Si_XGe_{(1-X)}$.

28. (Withdrawn) The imager of claim 26, wherein said silicon-germanium base layer comprises $Si_XGe_YC_Z$, and X+Y+Z = 1.

29. (Withdrawn) The imager of claim 26, wherein said silicon-germanium base layer has a germanium concentration of about 30% to about 40%.

30. (Withdrawn) The imager of claim 24, wherein said imager is a CMOS imager.

31. (Withdrawn) The imager of claim 24, wherein said at least one pixel cell further comprises a reset transistor, a source follower transistor, and row select transistor formed in regions of said substrate containing said strained layer.

32. (Withdrawn) The imager of claim 31, wherein said imager further comprises a transfer transistor formed in a region of said substrate containing said strained silicon layer.

33. (Withdrawn) The imager of claim 24, wherein said photosensor is a photodiode.

34. (Withdrawn) The imager of claim 24, wherein said at least one pixel cell is part of an imaging array.

35. (Withdrawn) A processing system comprising:

a processor;

an imaging device coupled to said processor, said imaging device having a plurality of pixel cells, at least one of said pixel cells comprising:

a semiconductor substrate including a strained silicon layer at an upper portion thereof;

a photosensor for generating charge formed in an upper region of said semiconductor substrate; and

a readout circuit comprising at least an output transistor formed on said substrate.

36. (Withdrawn) The system of claim 35, wherein said strained silicon layer has a thickness of about 500Å to about 1000Å.

37. (Withdrawn) The system of claim 35, wherein said strained silicon layer comprises a top silicon layer formed over a silicon-germanium layer.

38. (Withdrawn) The system of claim 37, wherein said silicon-germanium base layer has a germanium concentration of about 30% to about 40%.

39. (Original) A method of forming a pixel cell comprising:

forming a semiconductor substrate;

forming a strained silicon layer in association with an upper portion of said semiconductor substrate; and

forming a photosensor for generating charge at said upper portion of said semiconductor substrate.

40. (Withdrawn) The method according to claim 39, further comprising forming a reset transistor, a source follower transistor, and a row select transistor in regions of said substrate containing said strained layer.

41. (Withdrawn) The method according to claim 40, further comprising forming a transfer transistor in a region of said substrate containing said strained silicon layer.

42. (Original) The method according to claim 39, wherein said forming of a strained silicon layer is performed by forming a strained silicon layer having a thickness of about 500Å to about 1000Å.

43. (Original) The method according to claim 39, wherein said forming of a strained silicon layer is performed by forming a top silicon layer over a silicon-germanium base layer.

44. (Original) The method according to claim 43, wherein said silicon-germanium base layer comprises $Si_XGe_{(1-X)}$.

45. (Original) The method according to claim 43, wherein said silicon-germanium base layer comprises $Si_XGe_YC_Z$, and $X+Y+Z = 1$.

46. (Original) The method according to claim 43, wherein said step of forming said top silicon layer is performed by atomic layer deposition (ALD).

47. (Original) The method according to claim 43, wherein said step of forming said top silicon layer is performed by chemical vapor deposition (CVD).

48. (Original) The method according to claim 39, wherein said step of forming a strained silicon layer is performed by forming a top silicon layer over a silicon-germanium base layer having a germanium concentration of about 30% to about 40%.

49. (New) At least one pixel cell, comprising:

a semiconductor substrate including a strained silicon layer at an upper portion thereof;

a first charge collection region capable of collecting charge from impinging light formed below an upper surface of said strained silicon layer;

a second charge collection region for receiving charge from said first charge collection region, said second charge collection region formed below an upper surface of said strained silicon layer; and

a gate for electrically coupling said first and second charge collection regions, said gate being formed over said strained silicon layer.

50. (New) The pixel cell of claim 49, wherein said first charge collection region is formed entirely below a lower surface of said strained silicon layer.

51. (New) A method of forming a pixel cell, comprising:

forming a semiconductor substrate;

forming a strained silicon layer in association with an upper portion of said semiconductor substrate;

forming a first charge collection region capable of collecting charge from impinging light below an upper surface of said strained silicon layer;

forming a second charge collection region for receiving charge from said first charge collection region, said second charge collection region being formed below an upper surface of said strained silicon layer; and

forming a gate for electrically coupling said first and second charge collection regions over said strained silicon layer.

52. (New) The method according to claim 39, wherein said first charge collection region is formed entirely below a lower surface of said strained silicon layer.